A Low-Noise CMOS Image Sensor With Digital Correlated Multiple Sampling

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***Abstract*— This paper presents a low noise CMOS image sensor using conventional 3T active pixel with Nwell/Psub diode as photo detector. Both fixed pattern noise (FPN) and temporal noise are suppressed by the proposed digital correlated multiple sampling (DCMS) technology. FPN and temporal noise from pixel, buffer circuit, and column-parallel ADC are analyzed in detail, and the total noise with DCMS is derived. General expression of 1/f noise with correlated multiple sampling is given, illustrating impact of delay time in DCMS. Output noise of image sensor, frame rate, power, and area are affected by order and oversampling ratio of sigma–delta ADC, which are discussed for practical design. A prototype CMOS image sensor with 800×600 pixel array and second-order incremental sigma–delta ADCs is implemented with the 0.35-μm standard CMOS process. Measurement results of the implemented image sensor show a column FPN of 0.009%, an input referred noise of 3.5 e^-_{rms}, and a dynamic range of 84 dB with oversampling ratio of 255. This indicates that image sensor with low noise can be achieved by DCMS without the CIS process and column amplification.**

***Index Terms*— CMOS image sensor, sigma-delta ADC, low noise, FPN, digital correlated multiple sampling.**

I. Introduction

CMOS image sensor (CIS) for low-light level imaging is desirable in applications of scientific imaging, medical imaging and security. To achieve good imaging quality under low-illumination conditions, the CIS needs both low spatial noise and temporal noise.

High-gain column amplifier is helpful to reduce the temporal noise [1], but the uniformity of image is deteriorated due to the mismatch of devices in amplifier. The introduced column fixed pattern noise (FPN) corrupts the imaging quality more seriously at low light intensity than high light intensity. Correlated double sampling (CDS) [2], [3] can suppress offset FPN, low frequency noise and reset noise of pixel effectively by the correlation of reset voltage and integrated signal voltage. In addition, correlated multiple sampling (CMS) [4]–[6] is developed to reduce temporal noise further by average of multiple samples from these two voltage levels. The effect of CDS/CMS to low frequency noise is inversely proportional to the interval of two samples, thus floating diffusion output node is used in 4T pixel to realize the readout of reset voltage and signal voltage subsequently. This implementation is supplied by customized CIS process with option of pinned photodiode [7], which provides improved photo-responsivity and noise performance compared with standard PN junction.

However, CIS process with high performance is not available to common customers as the process parameters for pinned photodiode and other units in pixel are optimized by foundry for requirements of specific customers. The additional mask layers and process optimization increase cost further. Delta difference sampling (DDS) [7], [8] is proposed to improve the uniformity with standard CMOS process, which subtracts the integrated signal voltage in one frame and reset voltage in the following frame. Since the samples in different frames are un-correlated, the resulted reset noise power doubles.

To achieve low noise imaging with standard CMOS process, this paper presents a digital correlated multiple sampling (DCMS) technique for 3T pixel to suppress spatial noise as well as temporal noise without pinned photodiode. Compared with analog CDS, CMS and DDS, suffering from FPN of column-parallel ADC array, better uniformity can be obtained if the subtraction is executed in digital domain since FPN from all stages of image sensor is suppressed. The increased temporal noise due to the un-correlated noise sources is attenuated significantly by the multiple sampling and average of column-parallel sigma-delta ADC. Both Spatial noise and temporal noise from all noise sources of image sensor with proposed DCMS is analyzed in this paper, and the measurement results of prototype image sensor confirm the effectiveness of DCMS to FPN and temporal noise.

The paper is organized as follows: Section II describes the image sensor architecture and the proposed DCMS. FPN with DCMS is discussed in Section III, followed by temporal noise analysis of DCMS in detail in Section IV. Design of column-parallel sigma-delta ADC is presented in Section V. Section VI shows the implementation and measurement results, followed by the conclusion in Section VII.

II. Proposed DCMS and Architecture

Fig. 1 shows the architecture of the proposed CMOS image sensor. The image sensor consists of a 800×600 pixel array, column-parallel sigma-delta ADC array, digital column MUX circuits, row decoder and timing controller. The column readout circuits place on both top and down sides of the pixel array, and each side contains 400 columns. Off-chip buffer

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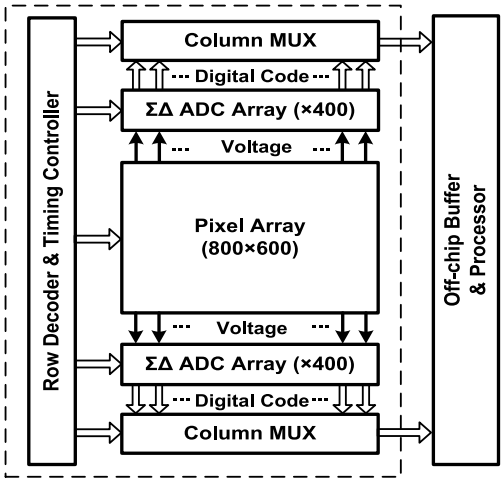

Fig. 1. Block diagram of the CMOS image sensor.

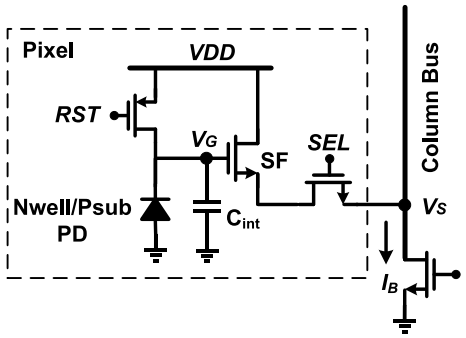

Fig. 2. Pixel circuit.

are used to realize the proposed DCMS operation. Rolling shutter is used for adequate integration time and simple pixel circuits. 3T active pixel structure is designed in the image sensor, as shown in Fig. 2, which uses Nwell/Psub diode instead of pinned photodiode.

The basic idea of DCMS is similar to CMS, while the sampling timing should be modified to be compatible with 3T pixel. The operation principle of DCMS is shown in Fig. 3. Rather than the adjacent sampling of reset and signal voltage in one pixel for CDS/CMS with 4T pixel, the proposed DCMS with 3T pixel has to sample reset voltage of all pixels and buffer their digital codes (D_R), then samples signal voltage and digitize as D_S. Both reset voltage and signal voltage are sampled with multiple times by column-parallel sigma-delta ADC in readout phase, and the output code (D_O) is obtained by the difference of signal code (D_S) and the buffered reset code (D_R) for each pixel. A frame buffer is required to store reset codes of all pixels for one frame, which will occupy considerable area if it is implemented on chip. Alternatively, off-chip memory is used to realize DCMS, taking the advance of high volume, high speed and low cost in advanced nano-meter CMOS technology for memory.

Note that there is no additional circuit between pixel output and input of ADC, especially the sampling and hold circuit before ADC is removed to take the advantage of time average

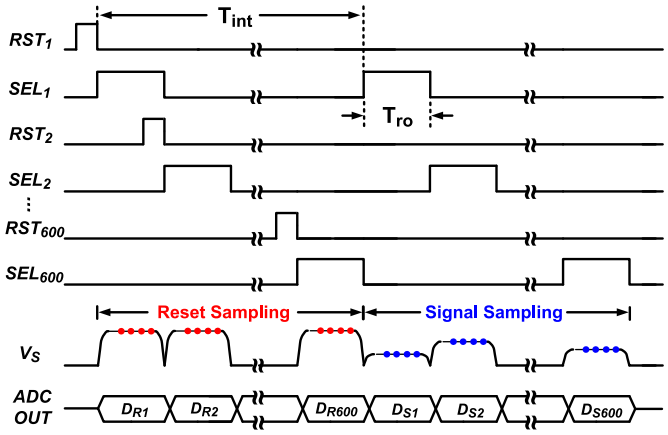

Fig. 3. Operation principle of proposed DCMS.

for noise reduction. This will cause voltage dropping of ADC input during sampling, since photo current is still integrating in this phase. As sigma-delta ADC outputs mean value for the dropping voltage during the whole sampling phase of one pixel, the result actually corresponds to the level integrated for T_{int} plus half time of readout phase (T_{ro}).

As shown in Fig. 2, the reset voltage of pixel is supply voltage (VDD), and the input voltage of source follower (NMOS) is

$$V_G = VDD - \frac{(I_{pd} + I_d)T'_{\text{int}}}{C_{\text{int}}} \tag{1}$$

where I_{pd} and I_d are photo current and dark current from photodiode, respectively. T'_{int} is the equivalent integration time as T_{int}=T_{int} + T_{ro}/ 2, and C_{int} is integration capacitance including junction capacitance and parasitic capacitance.

Supposing the source follower is in saturation and neglect influence of the switch controlled by SEL, the output voltage of pixel for integration time of T_{int} can be obtained as

$$V_S = V_G - V_{GS,SF} = VDD - \frac{(I_{pd} + I_d)T'_{int}}{C_{int}} - V_{TN} - \sqrt{\frac{2I_B}{\mu_N C_{ox} W_{SF}/L_{SF}}} \tag{2}$$

where V_{TN}, W_{SF} and L_{SF} are the threshold voltage, effective width and length of source follower, respectively. I_B is the bias current of source follower, μ_N is the mobility of NMOS, and C_{ox} is the gate oxide capacitance per unit area.

Digital output of Vs from L_{th}-rder incremental sigma-delta ADC with oversampling ratio of M is

$$\begin{aligned} D_S &= \frac{V_S - V_{OS}}{V_{REF}} \frac{1}{L!} \prod_{i=0}^{L-1} [c_i(M+i)] \\ &= \left[VDD - \frac{(I_{pd}+I_d)T'_{int}}{C_{int}} - V_{TN} - \sqrt{\frac{2I_B L_{SF}}{\mu_N C_{ox} W_{SF}}} - V_{OS} \right] \\ &\quad \times \frac{\prod_{i=0}^{L-1} [c_i(M+i)]}{V_{REF} L!} \end{aligned} \tag{3}$$

where c_i is gain of the i_{th} integrator in sigma-delta modulator, V_{REF} is reference voltage, and V_{OS} is offset voltage in ADC.

The integration time T'_{int} in (3) is zero for digital output of reset voltage V_R.

The final output with DCMS is

$$D_O = D_R - D_S = (V_R - V_S)\frac{\prod_{i=0}^{L-1}[c_i(M+i)]}{V_{REF}L!} = \left[\frac{(I_{pd}+I_d)T'_{\text{int}}}{C_{\text{int}}} + \Delta V_{TN}\right]\frac{\prod_{i=0}^{L-1}[c_i(M+i)]}{V_{REF}L!} \quad (4)$$

where ΔV_{TN} is the difference of source follower's threshold voltage between reset and signal sampling due to body effect.

III. FPN Analysis of DCMS

There are three types of noise that degrade the quality of image sensor. The first one is FPN caused by spatial non-uniformity, the second one is temporal noise due to photo detector and circuits in image sensor, and the third one comes from substrate and supply voltage fluctuations. Total random noise is composed of the last two types of noise. The last type noise is not discussed in the following analysis.

FPN comes from the mismatch of devices and process variation in space. Supposing that all the sources of spatial non-uniformity are uncorrelated, pixel FPN of signal sampling with normal operation can be derived from (3) as

$$\sigma^2_{pix} = \sigma^2_{I_{pd}} + \sigma^2_{I_d} + \sigma^2_{C_{int}} + \sigma^2_{V_{TN}} + \sigma^2_{W_{SF}} + \sigma^2_{L_{SF}} \quad (5)$$

where variations of photo current, dark current and integration capacitance lead to gain FPN, while non-uniformity from threshold voltage and dimension of source follower contribute to offset FPN.

Similarly, column FPN due to non-uniformity of column parallel circuits can be derived as

$$\sigma^2_{col} = \sigma^2_{I_B} + \sum_{i=0}^{L-1}\sigma^2_{C_i} + \sigma^2_{V_{OS}} \quad (6)$$

where variations of ADC gain results in gain FPN, while offset from bias current of source follower and ADC give rise to offset FPN.

According to (4), items not related to signal are cancelled by DCMS, and the consequent pixel FPN and column FPN are shown as follows, respectively.

$$\sigma^2_{pix,DCMS} = \sigma^2_{I_{pd}} + \sigma^2_{I_d} + \sigma^2_{C_{int}} + {\sigma'_{VTN}}^2 \quad (7)$$

$$\sigma^2_{col,DCMS} = \sum_{i=0}^{L-1}\sigma^2_{C_i} \quad (8)$$

Most offset FPN is eliminated by DCMS except residue variation of threshold voltage due to body effect. However gain FPN is not affected by DCMS or other double sampling techniques, which can be reduced by more complicated calibration technology [9], [10]. Compared with analog CDS, CMS or DDS, DCMS not only eliminates offset FPN from pixel circuits, but also cancels the spatial variation of column readout circuits including ADCs. Thus considerable improvement of FPN is expected with DCMS.

IV. Temporal Noise Analysis of DCMS

The source of temporal noise includes pixel circuits, buffer circuits and column circuits. In previous works [1], [11]–[14], analysis of temporal noise mainly focus on pixel and buffer circuits, however the impact of column-parallel ADC is not concerned. Noise from each source in image sensor and the total noise will be analyzed in the following. As the temporal noise is much smaller than signal, small signal circuit is used in the analysis.

A. Noise of Pixel

The reset operation of pixel introduces thermal noise, which noise power with reset switch of PMOS is well known as

$$\overline{V^2_{n,rst}} = \frac{kT}{C_{int}} \quad (9)$$

where k is the Boltzmann constant and T is the absolute temperature [12]. C_{int} is the integration capacitance given by

$$C_{int} = C_{pd} + (1 - A_{SF})C_{gs,SF} \quad (10)$$

where C_{pd} is the capacitance of photo detector, $C_{gs,SF}$ is the gate-source capacitance of source follower, andA_{SF} is the voltage gain of source follower as

$$A_{SF} = \frac{\partial V_S}{\partial V_G} = \frac{g_{m,SF}}{g_{m,SF} + g_{mb,SF}} = \frac{1}{1+\eta} \quad (11)$$

where $g_{m,SF}$ is the transconductance of source follower, $g_{mb,SF}$ is the transconductance due to body effect, and $\eta = g_{mb,SF}/g_{m,SF}$ for source follower in saturation.

Reset noise at column bus becomes

$$\overline{V^2_{n,RST}} = A^2_{SF}\overline{V^2_{n,rst}} = \frac{kT}{C_{int}(1+\eta)^2} \quad (12)$$

Photo current I_{pd} and dark current I_d of photodiode introduce shot noise with the following PSD

$$S_{I,shot} = q(I_{ph} + I_d) \quad (13)$$

where q is the charge of electron. After integration with time T_{int}, the noise voltage at column bus is

$$\overline{V^2_{n,shot}} = A^2_{SF}\int_0^{T_{int}}\frac{S_{I,shot}}{C^2_{int}}dt = \frac{q(I_{pd}+I_d)T_{int}}{C^2_{int}(1+\eta)^2} \quad (14)$$

B. Noise of Buffer

When the pixel is selected to read out, its source follower and the current bias transistor contribute thermal noise with the following PSD [15], where the noise of switching transistor is ignored.

$$S_I = 4kT\gamma g_m \quad (15)$$

where γ is the excess noise factor given by 2/3, and g_m is the transconductance of source follower or current bias transistor.

Small signal model for noise analysis of buffer is shown in Fig. 4. The resistance of current bias transistor is R_B=$1/g_{ds,B}$. The transconductance from source voltage of source follower to its drain current is

$$G_{SF} = \frac{\partial I_{DS}}{\partial V_S} = g_{m,SF}\frac{C_{pd}}{C_{pd} + C_{gs,SF}} \quad (16)$$

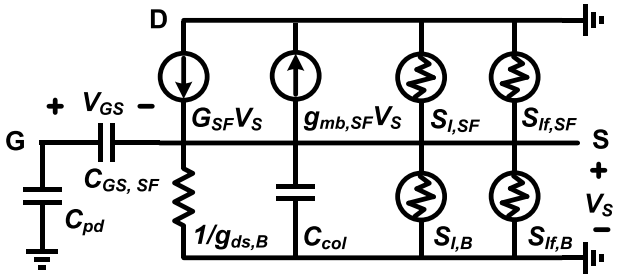

Fig. 4. Small signal model for noise analysis of source follower and current bias transistor.

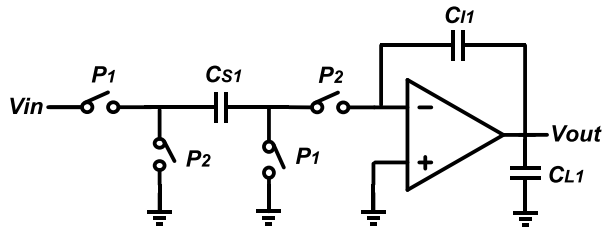

Fig. 5. Integrator circuit of sigma-delta modulator.

Then the equivalent resistance of source follower is given by

$$R_{SF} = \frac{1}{g_{mb,SF} + G_{SF}} = \frac{1}{\alpha g_{m,YSF}} \tag{17}$$

where α is the coefficient defined as

$$\alpha = \eta + \frac{C_{pd}}{C_{pd} + C_{gs,SF}} \tag{18}$$

Capacitance of column bus C_{col} forms low-pass filter with R_{SF} and R_B, and the noise transfer function is

$$H_{BUF}(f) = \frac{1}{1 + j2\pi f C_{col}(R_{SF}//R_B)} = \frac{1}{1 + \frac{j2\pi f C_{col}}{\alpha g_{m,SF} + g_{ds,B}}} \tag{19}$$

Now thermal noise power of buffer can be derived as

$$\begin{aligned}\overline{V_{n,BUF}^2} &= \int_0^\infty \left(S_{I,SF}R_{SF}^2 + S_{I,B}R_B^2\right)|H_{BUF}(f)|^2 df \\ &= \frac{kT\gamma\,(\alpha g_{m,SF} + g_{ds,B})}{C_{col}}\left(\frac{1}{\alpha^2 g_{m,SF}} + \frac{g_{m,B}}{g_{ds,B}^2}\right)\end{aligned} \tag{20}$$

C. Noise of Column-parallel ADC

In the proposed architecture, column readout path only has sigma-delta ADC, thus there is no additional column circuit adding readout noise. Thermal noise and 1/f noise from integrators of sigma-delta modulator, as well as quantization error contribute the noise of ADC.

Each integrator in sigma-delta modulator contributes noise to the total output noise, but we only consider the first integrator's influence here because the noise from subsequent integrators is attenuated by high pass response. The integrator is implemented by switched capacitor and amplifier as shown in Fig. 5, which model for noise analysis is shown in Fig. 6.

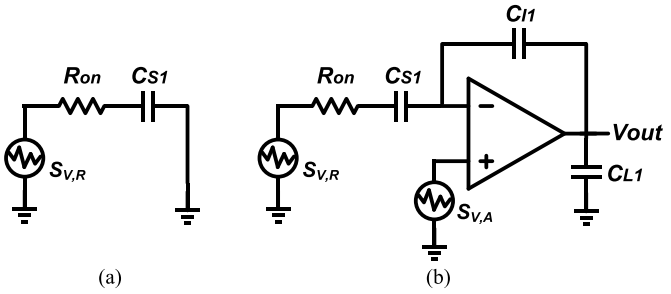

Fig. 6. Noise analysis model of integrator in (a) sampling phase and (b) integration phase.

In sampling phase ($P_1 = 1$, $P_2 = 0$), the switched-capacitor circuits introduce kT/C noise. Since the noise is aliased to the band from 0 to Nyquist frequency, the noise PSD is given by

$$S_{V,SW} \approx \frac{2kT}{C_{S1} f_s} \tag{21}$$

where C_{S1} is the sampling capacitance of the first integrator.

In integration phase (P_1 =0, P_2 =1), both switches and amplifier contribute noise. Foldover of amplifier's thermal noise should be considered in sampling system, and this effect can be approximated by $f_{Bn}/(f_s/2)$ [16], where f_{Bn} is the equivalent noise bandwidth as

$$f_{Bn} = \frac{\pi}{2} GBW_{A1} = \frac{g_{m,A1}}{4C_{P2}} \tag{22}$$

where GBW_{A1} is the gain-bandwidth product of amplifier, and $g_{m,A1}$ is the transconductance of input transistor. C_{P2} is the compensation capacitance for two-stage amplifier, while it is the output capacitance of amplifier for one-stage amplifier as

$$C_{P2} = \frac{C_{S1}C_{I1}}{C_{S1} + C_{I1}} + C_{L1} \tag{23}$$

where C_{I1} and C_{L1} are integration capacitance and load capacitance of the first integrator.

Input referred noise of amplifier is related to its specific topology, which can be derived with small signal model. With no loss of generality, we suppose that the thermal noise of amplifier is dominated by its input transistor, then the noise PSD of amplifier is

$$\begin{aligned}S_{V,A} &= \frac{4kT\gamma}{g_{m,A1}}\frac{2f_{Bn}}{f_s} + \frac{K_f}{C_{ox}^2(WL)_{A1}}\frac{1}{f} \\ &= \frac{2kT\gamma}{f_s C_{P2}} + \frac{K_f}{C_{ox}^2(WL)_{A1}}\frac{1}{f}\end{aligned} \tag{24}$$

in which the first component is thermal noise, and the rest is $1/f$ noise. K_f is the flicker noise parameter with 10^{-31} $\mathrm{F^2V^2/cm^2}$, W and L are effective width and length of transistor, respectively.

The noise of sigma-delta modulator is derived as

$$\begin{aligned}\overline{V_{n,MOD}^2} &= \int_0^{f_B} (2S_{V,SW} + S_{V,A})df \\ &= 2kT\left(\frac{2}{C_{S1}} + \frac{\gamma}{C_{P2}}\right)\frac{f_B}{f_s} + \frac{K_f}{C_{ox}^2(WL)_{A1}}\ln f_B\end{aligned} \tag{25}$$

where $1/f$ noise is integrated from 1 Hz instead of 0. Note that oversampling ratio is $M = fs/(2fB)$, and scanning frequency of row fits $f_0 = 2f_B$, then the noise power becomes

$$\overline{V_{n,MOD}^2}(M) = \frac{kT}{M}\left(\frac{2}{C_{S1}} + \frac{\gamma}{C_{P2}}\right) + \frac{K_f}{C_{ox}^2(WL)_{A1}} \ln\left(\frac{f_0}{2}\right) \tag{26}$$

Thermal noise of modulator is suppressed by M, while $1/f$ noise cannot be reduced by oversampling as it is low frequency noise. It is clear that large sampling capacitance is desirable for low noise of modulator, whereas large capacitance will give rise to reduction of gain-bandwidth product and increase of power dissipation.

To reduce total noise of image sensor, $1/f$ noise of ADC should be minimized. With the parameters will be given in Part F, thermal noise of modulator is about 18 μV with $M = 250$, while $1/f$ noise is up to 54 μV for input transistor with minimum dimension in 0.35-μm process. Transistor with large dimension is a simple way to reduce $1/f$ noise. For example, if area of input transistor becomes 600 times of the minimum one, $1/f$ noise would decrease to 2 μV. It is a practical solution in this design because of the relative large width of ADC (32 μm), whereas it is not available for small pixel pitch, such as 1 or 2-μm pitch for high resolution imager. For ADC with smaller width, further techniques are required to minimize its $1/f$ noise. Autozero has been implemented in 12-bit sigma-delta ADC with 0.13-μm process to reduce $1/f$ noise and offset, by which image sensor with 2.25μm pixel pitch achieves temporal noise of 2.4 e^-_{rms} [6]. Chopper stabilization is another effective way by modulation rather than sampling, which has been successfully utilized in [17] for 15-bit incremental sigma-delta ADC.

Quantization noise is caused by the quantization error as [18]

$$S_{V,Q} = \frac{\Delta^2}{12f_s} = \frac{1}{12f_s}\left(\frac{V_{REF}}{2^N}\right)^2 \tag{27}$$

where Δ is the LSB of ADC determined by the reference voltage (V_{REF}) and resolution (N).

The noise transfer function of L_{th}-order modulator with single bit quantization is

$$NTF(z) = (1 - z^{-1})^L\Big|_{z=j2\pi f/f_s} \approx \left(\frac{j2\pi f}{f_s}\right)^L \tag{28}$$

The quantization noise power is derived as

$$\begin{aligned}\overline{V_{n,Q}^2}(M, L) &= \int_{-f_B}^{f_B} S_{V,Q}\,|NTF(f)|^2 df \\ &\approx \frac{1}{12}\left(\frac{V_{ref}}{2^N}\right)^2 \frac{\pi^{2L}}{(2L+1)M^{2L+1}}\end{aligned} \tag{29}$$

The calculated quantization noise for first to fourth-order modulators with different oversampling ratio are shown in Fig. 7. Compared to thermal noise of integrator only attenuated by oversampling, quantization noise is suppressed further more by noise shaping, thus high resolution can be achieved with high order modulation or large oversampling ratio. Large oversampling ratio (over 500) is needed for low quantization noise in first-order modulator due to its weak noise shaping, while oversampling ratio can be reduced significantly for second-order or higher order modulator with enhanced noise shaping.

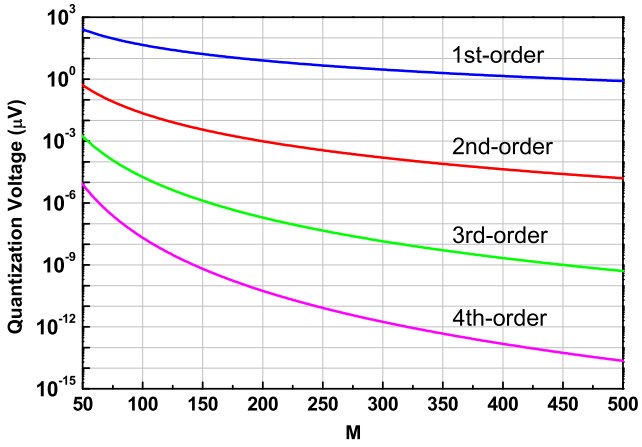

Fig. 7. Estimated quantization noise for sigma-delta ADC with different order.

D. Thermal Noise with DCMS

Thermal noise of ADC and its input noise including shot noise and thermal noise of buffer are suppressed by the multiple sampling and average of sigma-delta ADC, and the output noise is influenced by impulse response of decimation filter as

$$\overline{V_{n,out}^2} = \overline{V_{n,in}^2} H_{dec}(L) \tag{30}$$

The cascaded digital integrators are used as decimation filter of incremental sigma-delta ADC for the reason of power and area, which impulse response of L_{th}-order filer is

$$H_{dec}(L) = \sum_{i=1}^{M} w_i^2(L) \tag{31}$$

where w_i (L) is the weight coefficients of the L_{th}-order decimation filter for the i_{th} cycle. The weight coefficients are $1/M$ for the first-order filter, while they are cycle dependent for higher order filters [19]. w_i of L_{th}-order decimation filter is found by

$$w_i(L) = \frac{L\prod_{j=1}^{L-1}(M + j - i)}{\prod_{j=0}^{L-1}(M + j)} \tag{32}$$

The corresponding impulse response can be derived by (31) and (32) as

$$H_{dec}(L) \approx \frac{L^2}{(2L-1)M} \tag{33}$$

Thus H_{dec} of first to fourth-order decimation filters are $1/M$, $4/(3M)$, $9/(5M)$ and $16/(7M)$, respectively. Note that the low frequency noise, such as 1/f noise, will not be influenced by above effect.

The reset noise in samples of reset and signal with DCMS are fully correlated, thus they can be canceled. However other thermal noise power excepting shot noise will double as they have no correlation. The resulted output thermal noise power with DCMS is

$$\overline{V_{n,out}^2} = 2\overline{V_{n,in}^2} H_{dec}(L) \tag{34}$$

E. 1/f Noise With DCMS

$1/f$ noise from ADC can be ignored by techniques mentioned above, whereas the component from pixel buffer should be taken into account even with DCMS. The analysis of $1/f$ noise is more complex as it is not fully correlated in different samples of DCMS.

$1/f$ noise PSD of transistor is given by

$$S_{If} = \frac{K_f g_m^2}{C_{ox}^2 WL} \frac{1}{f} \tag{35}$$

and $1/f$ noise PSD of pixel buffer is

$$\begin{aligned} S_{Vf} &= \left(S_{If,SF} R_{SF}^2 + S_{If,B} R_B^2\right) \\ &= \frac{K_f}{2C_{ox}^2} \left(\frac{1}{\alpha^2 W_{SF} L_{SF}} + \frac{g_{m,B}^2}{g_{ds,B}^2 W_B L_B}\right) \frac{1}{f} \end{aligned} \tag{36}$$

According to Fig. 3, voltage difference of reset sampling and signal sampling is

$$\Delta V_S = \frac{1}{M} \left[\sum_{i=0}^{M-1} V_S(iT_s) - \sum_{i=0}^{M-1} V_S(iT_s - T_{int})\right] \tag{37}$$

where T_s is the sampling period of ADC ($T_s = 1/f_s$), M is oversampling ratio, and T_{int} is the delay between samples of reset and signal. Considering $T_{int} = N_r M T_s$, noise transfer function of CMS can be derived according to [11] as

$$|H_{CMS}(x)|^2 = \frac{4\sin^2(x)\sin^2(xN_r)}{M^2 \sin^2(\frac{x}{M})} \tag{38}$$

where $x = \omega M T_s/2$. Now output $1/f$ noise power is obtained as

$$\begin{aligned} \overline{V_{nf,BUF}^2}(M) &= \int_0^\infty S_{Vf} \frac{|H_{CMS}(x)|^2}{1 + (\frac{\omega}{\omega_c})^2} dx \\ &= \frac{N_f}{M^2} \int_0^\infty \frac{4\sin^2(x)\sin^2(xN_r)}{x \sin^2(\frac{x}{M}) \left[1 + (\frac{x}{Mx_c})^2\right]} dx \end{aligned} \tag{39}$$

where $x_c = \omega_c T_s/2$, and ω_c is the cut-off angular frequency. N_f is the relative magnitude of $1/f$ noise power as

$$N_f = \frac{K_f}{2C_{ox}^2} \left(\frac{1}{\alpha^2 W_{SF} L_{SF}} + \frac{g_{m,B}^2}{g_{ds,B}^2 W_B L_B}\right) \tag{40}$$

Equation (39) is the general expression of $1/f$ noise power from pixel buffer with CMS, being valid for both 3T and 4T pixels. $N_r = 1$ corresponds to CMS with 4T pixel, while N_r must be equal to row number of pixel array at least for 3T pixel with the proposed DCMS. $M = 1$ is the case of CDS, and for $M \to \infty$, the noise power becomes

$$\begin{aligned} \overline{V_{nf,BUF}^2}(\infty) &= N_f \int_0^\infty \frac{4\sin^2(x)\sin^2((xN_r)}{x^3} dx \\ &= N_f[(N_r - 1)^2 \ln(N_r - 1) - 2(N_r)^2 \ln(N_r) \\ &\quad + (N_r + 1)^2 \ln(N_r + 1)] \end{aligned} \tag{41}$$

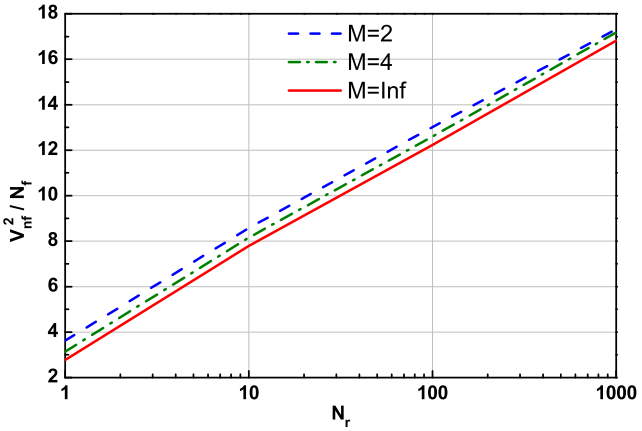

Fig. 8. Normalized 1/f noise power with CMS.

To evaluate the impact of delay time between samples of reset and signal, normalized $1/f$ noise power by numerical calculation from (39) is shown in Fig. 8, in which $\omega_c T_s = 6$. $1/f$ noise increases considerably with longer delay time, thus minimum noise is obtained with $N_r = 1$, corresponding to 4T pixel. Effect of oversampling ratio M is also evaluated, which does not help much for the reduction of $1/f$ noise when N_r is large, whereas 70% of $1/f$ noise power can be reduced by CMS compared with CDS for $N_r = 1$. It is found that when $M \geq 50$, simple calculation with (41) is adequate to predict $1/f$ noise power instead of (39), which is not related to cut-off frequency (ω_c) and sampling period (T_s). N_r is 600 in this design, thus normalized $1/f$ noise power is 15.6 with DCMS. Obviously, $1/f$ noise is the main limitation of 3T pixel to achieve lower noise even with the proposed DCMS, therefore relative large pixel pitch is preferred to compensate the degradation of $1/f$ noise performance in 3T pixel.

F. Total Noise

The total output noise power is given by

$$\overline{V_{n,out}^2} = \int_0^\infty \left[\sum_i^{S_i(f)|H_i(f)|^2}\right] df \tag{42}$$

where $S_i(f)$ is PSD of the i_{th} noise source, and$H_i(f)$ is noise transfer function from the i_{th} source to output. It's assumed that the noise from different sources are un-correlated, thus the total output noise power can be calculated by the summation of noise power from all sources as

$$\overline{V_{n,out}^2} = \sum_i \left\{\int_0^\infty \left[S_i(f)\,|H_i(f)|^2\right] df\right\} = \sum_i \overline{V_{n,i}^2} \tag{43}$$

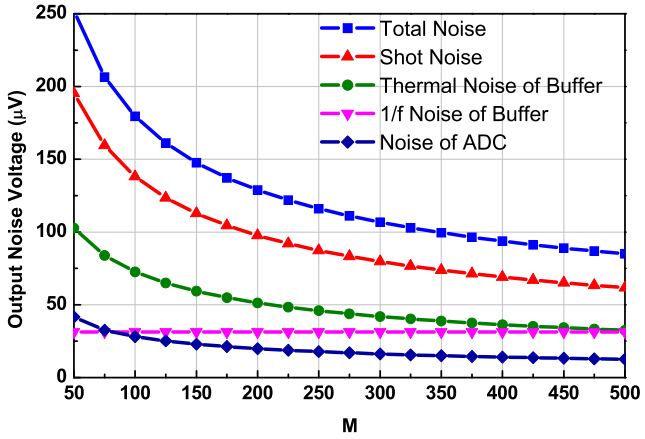

Fig. 9. Estimated noise voltage from different sources with multiple sampling for first-order sigma-delta ADC.

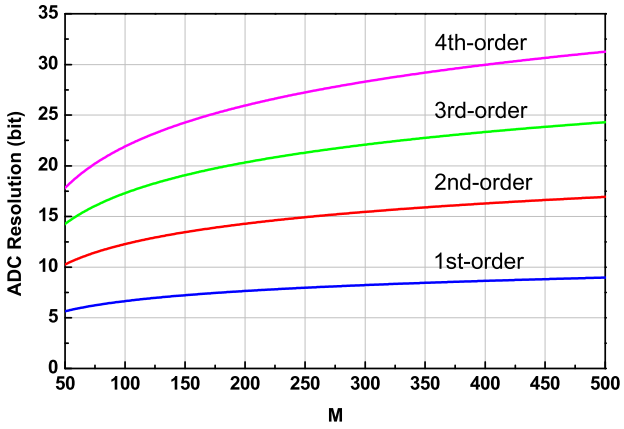

Fig. 10. Resolution of ADC with different order and oversampling ratio.

For simplicity, shot noise in reset sampling is ignored since its integration time is as short as 1/600 of signal sampling in this design. According to previous discussion, $1/f$ noise from sigma-delta modulator is also neglected, and the resulted output noise power with DCMS is

$$\overline{V_{n,out}^2} = 2H_{dec}(L)\left(\overline{V_{n,BUF}^2} + \overline{V_{n,MOD}^2}(1) + M\overline{V_{n,Q}^2}(M,L)\right) + H_{dec}(L)\overline{V_{n,SHOT}^2} + \overline{V_{nf,BUF}^2}(\infty) \quad (44)$$

in which $1/f$ noise of buffer is predicted with equation (41) as oversampling ratio of sigma-delta ADC is over 50 for gray scale of vision with 10 bits at least.

The conversion gain is

$$CG = \frac{qA_{SF}}{C_{int}} = \frac{q}{(1+\eta)C_{int}} \quad (45)$$

The input referred noise electron can be obtained by output noise voltage over CG as following

$$\overline{e_n} = \frac{\sqrt{\overline{V_{n,out}^2}}}{CG} = \frac{(1+\eta)C_{int}}{q}\sqrt{\overline{V_{n,out}^2}} \quad (46)$$

The estimated noise voltage from each source with multiple sampling of second-order sigma-delta ADC are shown in Fig. 9, as well as the total output noise of DCMS. The main parameters are $C_{int} = 4$ fF, $C_{col} = 5.37$ pF, $g_{m,SF} = 115.5$ μS, $g_{m,IB} = 105.5$ μS, $I_d + I_{pd} = 4.5$ fA, $C_{s1} = 200$ fF, $T_{int} = 50$ ms. The resulted conversion gain is 32 μV/e-. Obviously all the thermal noise are reduced effectively by multiple sampling, while 1/f noise from buffer circuits cannot be suppressed by this way. Shot noise is proportional to photo current, and it will be less than buffer's noise if photo current is smaller than 2 fA with above design parameters. Decrease rate of total noise will be lower in dark due to lack of shot noise. Noise contribution of ADC can be reduced to a low level at the cost of increased power and area according to (26).

V. ADC Design

Incremental sigma-delta ADC is very attractive in low noise application for its oversampling and noise shaping, as well as the immunity to non-idealities of analog circuits [19]. Thus we choose it as column-parallel ADC for DCMS. Besides output noise, power consumption and area must be also considered in the design of ADC because column-parallel ADC array usually dominates the total power of image sensor, while its width is limited by the pixel pitch.

A. Order of Modulation

Trade-off of oversampling ratio, frame rate, output noise, stability, power and area should be taken into account for the order of sigma-delta ADC.

Assuming that all the integrators in modulator are with unity gain, the resolution of L_{th}-order incremental sigma-delta ADC can be found by

$$N = \log_2\left[\frac{1}{L!}\prod_{i=0}^{L-1}(M+i)\right] \quad (47)$$

The resolution is determined by order of modulation L and oversampling ratio M. As shown in Fig. 10, large M is preferred to achieve low noise, at the cost of reduced bandwidth and frame rate. The image sensor needs at least 10-bit output for the gray scale of vision, thus ADC with first-order fails to effectively trade-off between resolution and frame rate. High-order modulation should be considered.

The input referred noise with DCMS for different orders of decimation filer (cascaded digital integrators) are estimated in Fig. 11. For reasons of power and area, decimation filter is designed with same order as modulator [19]. Compared with second-order filter, the noise increases by 40% and 80% for third and fourth-order, respectively. This is caused by the increased impulse response with high-order decimation filter, as shown in (33). In addition, more power and area are inevitable with increased integrators for higher-order ADC.

Stability is another factor of sigma-delta ADC design, which is degraded for higher-order modulation. For stable operation, the maximum input range of a second-order modulator is around 90% of reference voltage, while it is less than 75% in third-order one. The reduced input range would limit dynamic range of image sensor if third or higher-order modulator is used.

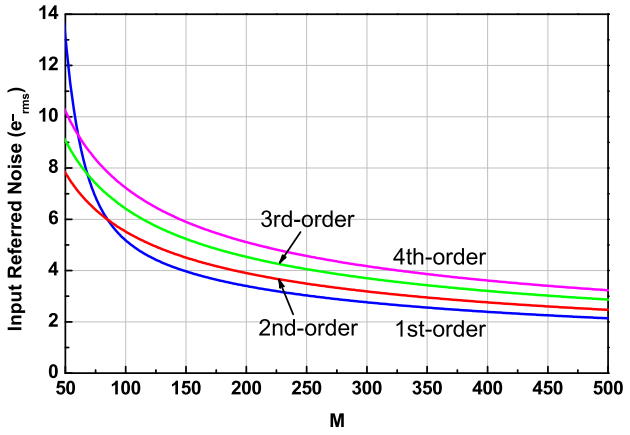

Fig. 11. Estimated input referred noise for different order sigma-delta ADC.

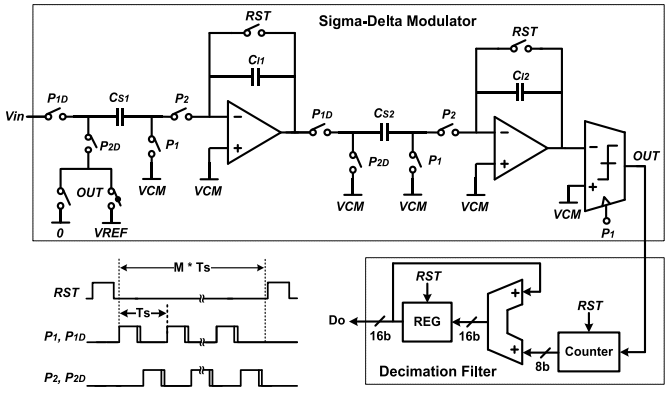

Fig. 12. Schematic of incremental sigma-delta ADC and timing diagram.

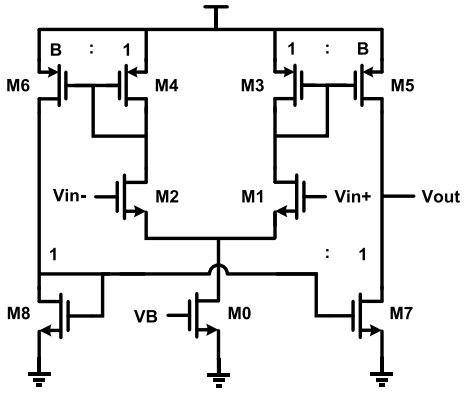

Fig. 13. Schematic of current mirror amplifier.

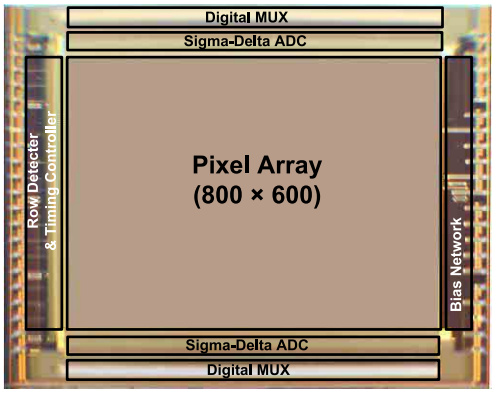

Fig. 14. Chip micrograph of the image sensor.

Based on above discussion, second-order sigma-delta ADC is a good choice for the trade-off of noise, stability, power and area. As far as frame rate is concerned, too large oversampling ratio is not practical, therefore M $\leq$ 300 is preferred in the design.

B. Circuits Design

Schematic of second-order incremental sigma-delta ADC is illustrated in Fig. 12. Sigma-delta modulator with single loop and single bit is preferred for efficiency of power and area. To be compatible with pixel output, single-end input is used rather than differential configuration. The maximum oversampling ratio is 255 in this design for 15-bit resolution.

Integrators in modulator are realized with switched-capacitor. They are reset at the beginning of each conversion period, then M cycles are run for one conversion. To avoid the signal-dependent charge injection, non-overlapping clocks with delayed falling edges are used in the integrators. All the clocks are supplied by the clock generator.

For incremental sigma-delta ADC, its decimation filter can be implemented by two cascaded digital integrators for second-order modulator [19]. The simplified circuits lead to considerable reduction of area and power compared with filters in normal sigma-delta ADC. As the modulator is 1-bit quantization, the first digital integrator can be implemented by simple ripple counter with 8 bits for $M \leq 255$. The second integrator is realized by 16-bit accumulator for 15-bit ADC resolution with 1-bit redundancy, which consists of adders and registers.

The first amplifier in modulator is critical as its noise cannot be suppressed by noise shaping, thus it usually dominates the main power consumption of modulator. Inverter has been used as amplifier in sigma-delta ADC for low power, whereas special techniques are required to compensate its poor PSRR and voltage offset [6]. For the same gain-bandwidth product and over drive voltage, current mirror amplifier is more power efficient than two-stage amplifier since no power is wasted in driving the compensation capacitance [20]. Therefore current mirror amplifier is used in this design, which schematic is shown in Fig. 13. The thermal noise of current mirror amplifier is given by

$$S_{V,A} = \frac{4kT\gamma}{g_{m1}}\left(1 + \frac{g_{m3}}{g_{m1}} + \frac{g_{m5}+g_{m7}}{g_{m1}}\right)\frac{2f_{Bn}}{f_s} \qquad (48)$$

which will replace (24) for noise estimation.

VI. Measurement Results

The prototype chip of proposed image sensor is fabricated with 1P4M 0.35-μm standard CMOS technology. The chip micrograph is shown in Fig. 14, which area is 16.4×13.5 mm^2. The pixel array is 800×600 with 16-μm pixel pitch, which

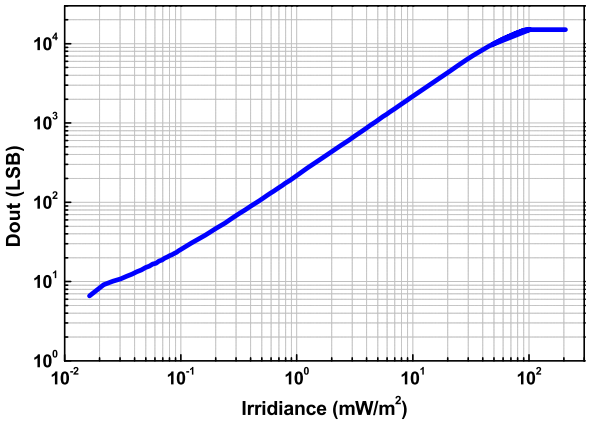

Fig. 15. Measured output code of image sensor versus light irradiance.

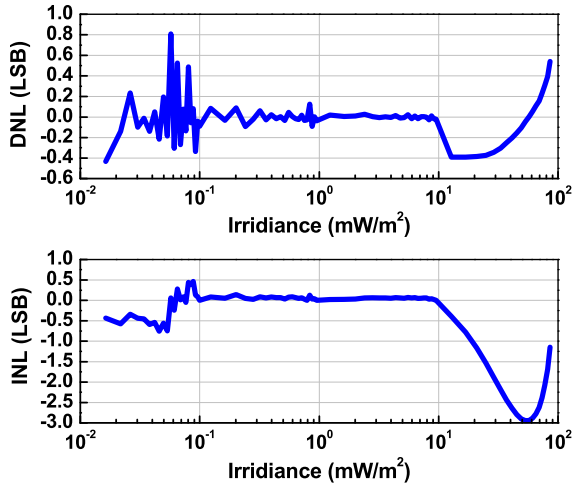

Fig. 16. Measured DNL and INL of the image sensor.

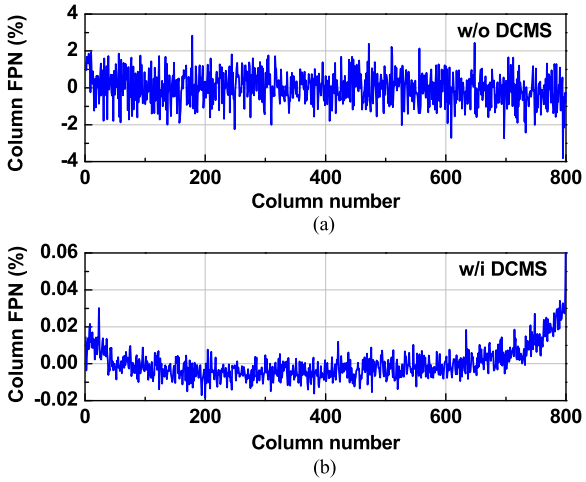

Fig. 17. Measured averaged column FPN (a) without DCMS and (b) with DCMS.

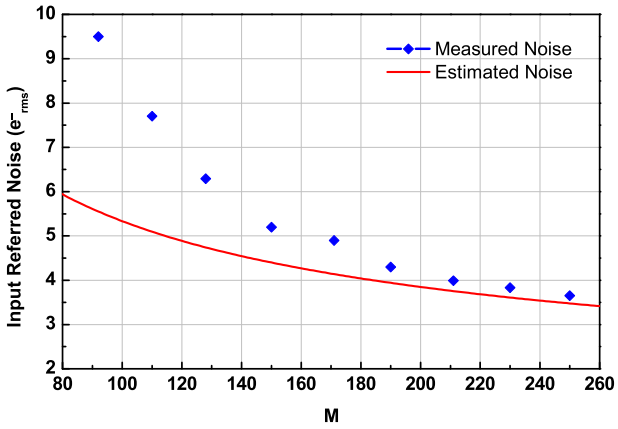

Fig. 18. Measured and estimated input referred noise with different oversampling ratio.

photo detector is implemented by Nwell/Psub diode rather than pinned photodiode. The output data are transmitted by two LVDS channels on top and down sides of pixel array.

One column-parallel ADC occupies 32×750 μm^2. Its sampling frequency is up to 7.8 MHz for maximum frame rate of 50 fps, and the power consumption of one ADC is 122 μW.

Fig. 15 shows the measured output code of image sensor with DCMS versus the light irradiance varying from 0.016 mW/m^2 to 210 mW/m^2, with oversampling ratio of 255. The maximum non-saturated output code is 14890 LSB, corresponding to full well capacity of 59 ke$^-$. Based on the curve in Fig. 15, non-linearity of the image sensor is shown in Fig. 16, which contains the non-linearity from integration-node capacitance, source follower of pixel and ADC. As illustrated in Fig. 16, the differential nonlinearity (DNL) of the proposed image sensor is within $+0.8/-0.4$ LSB. When irradiance is between $0.1\sim10$ mW/m^2, the DNL is within $+0.13/-0.09$ LSB, while the linearity will degrade for irradiance out of this range. The integration capacitance mainly comes from the junction capacitance of MOSFET, thus it changes obviously when the MOSFET leaves strong inversion region with low gate-source voltage, leading to worse linearity under high illuminance. On the other hand, the maximum linear input range of second-order sigma-delta ADC is less than 90% of its reference voltage, thus the linearity of image sensor at low light level is limited by ADC. The integral nonlinearity (INL) is within $+0.5/-3$ LSB as shown in Fig. 16, corresponding to 0.02% nonlinearity.

The measured averaged column FPN without and with DCMS at dark condition are shown in Fig. 17. The averaged column FPN is the averaged code of each column minus the mean value of all pixels, then over the maximum output code. The measured column FPN (rms) without DCMS is 0.85%, while it reduces to 0.009% with DCMS. The pixel FPN (rms) at dark condition are also measured, which is suppressed from 1.34% to 0.11% with DCMS. Thus the spatial uniformity is improved significantly by DCMS.

The temporal noise is measured for different oversampling ratio M with integration time of 60 ms. As shown in Fig. 18, the input referred noise with DDSM is measured at dark condition, and the estimated results from section IV are also given. The reduction of measured noise is more severe than estimated for small oversampling ratio, which is due to that the noise coupled from power supply, reference voltage and

TABLE I
PERFORMANCE COMPARISON WITH PREVIOUS WORK

Reference	[2] JSSC-11	[3] JSSC-13	[5] JSSC-12	[4] JS-12	[8] TBCS-11	[22] TCSI-15	This work
Process (μm)	0.13 μm CIS	0.15 μm CIS	0.18 μm CIS	0.18 μm CIS	0.5 μm sd.CMOS	0.13 μm CIS	0.35 μm sd.CMOS
Pixel number	2.1M	66k	1M	14	16.4k	316k	480k
Pitch (μm)	2.25	5.5	7.5	10	20.1	5.6	16
Pixel type (Photodiode)	4T-APS (PPD)	4T-APS (PPD)	4T-APS (PPD)	4T-APS (PPD)	CTIA (NPD)	4T-APS (PPD)	3T-APS (NPD)
Noise reduction technique	A. CDS	D. CDS	CMS	CMS Col. Amp.	A. DDS	D. CDS Col. Amp.	DCMS
ADC type	Cyclic	ΣΔ	FI-Cyclic	SS	Off-chip	SAR+ΣΔ	ΣΔ
ADC resolution (bit)	10	12	13-19	10/12	Off-chip	12	15
Temporal noise (e^-_{rms})	12.5	18.4	1.2	2.8*	26	18.6/2.5**	3.5
Column FPN (rms)	0.1%	0.014%	0.004%	N.A.	N.A.	0.4%	0.009%
CG (μV/e^-)	80	20	67	45	32	43	32
Intrascene DR (dB)	59	63	82	67	44	64	84
Max. frame rate (fps)	250	120	50	N.A.	70	6.8/150	50
Power (mW)	300	93	450	N.A.	2.37***	N.A.	193

*Measured with 12× analog gain. **Measured with 8× analog gain. ***Measured without ADC.

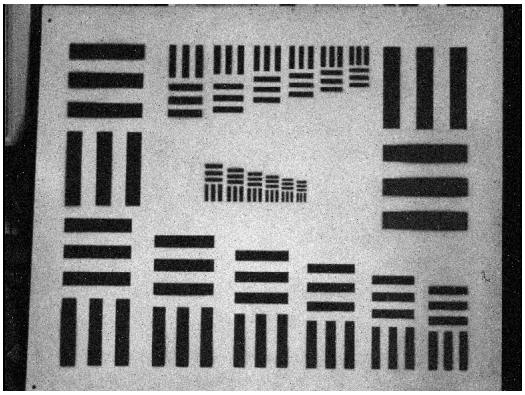

Fig. 19. Sample image with the implemented image sensor at 0.3 lux.

substrate dominate total noise [5]. They are not considered in the analysis of Section IV, which noise power are attenuated more drastically with $1/M^2$ by noise shaping in sigma-delta ADC [21]. When M increases over 180 (according to 14 bits for second-order sigma-delta ADC), the coupled noise are attenuated to a low level and temporal noise from circuits of image sensor dominate the total random noise, thus good agreement between measurement and estimation is exhibited. For 15-bit resolution ($M = 255$) in this design, the measured input referred noise with DCMS is 3.5 e^-_{rms}(112 μV).

Fig. 19 shows the sample image with the implemented image sensor at low-light level of 0.3 lux, and the oversampling ratio is 255 at frame rate of 16 fps. To reduce dark current, the sample image is obtained by cancellation from the image at dark with same integration time.

The performance comparison with previous works is listed in TABLE I. Nwell/Psub diode (NPD) in standard (sd.) CMOS process is used as photo detector in [8] and this work, while other works in the table utilize pinned photodiode (PPD) in CMOS image sensor (CIS) process. The proposed image sensor is measured with oversampling ratio of 255. Image sensor with DCMS achieves both low spatial and temporal noise even without 4T pixel and pinned photodiode. The comparison shows that DCMS suppresses noise more effectively than analog/digital CDS and DDS without column amplification.

VII. CONCLUSION

A low noise CMOS image sensor with digital correlated multiple sampling is proposed in this paper. Rather than pinned photodiode in CIS process, Nwell/Psub diode in standard CMOS process is used to reduce cost. Very low column FPN is achieved by the DCMS operation. Temporal noise of image sensor with DCMS is analyzed, in particular the general $1/f$ noise expression with CDS/CMS is illustrated. The measured low noise performance confirms the effectiveness of proposed DCMS for 3T pixel. Small conversion gain of 3T pixel and degradation of $1/f$ noise due to long delay between samples in DCMS are main limitations of 3T pixel and the proposed DCMS to achieve lower input referred noise. Large pixel pitch is helpful to minimize $1/f$ noise, whereas it is not feasible for high resolution imager. Anyway, DCMS supplies a solution for low-noise image sensor even without CIS process and column amplification.

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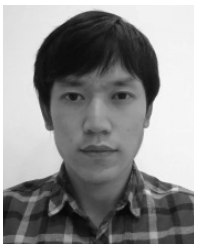

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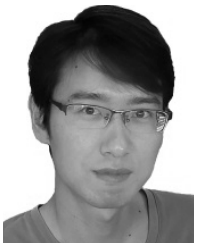

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